Course Number and Name

BEC015 - ASIC DESIGN

Credits and Contact Hours

3 and 45

Course Coordinator's Name

Ms G.Meena Kumari

Text Books and References

Course Description

- To acquire knowledge about different types of ASICs design.
- To study about various types of Programmable ASICs architectures and interconnects

Prerequisites	Co-requisites
Principles of Digital Electronics	Nil

required, elective, or selected elective (as per Table 5-1)

Selected Elective

Course Outcomes (COs)

CO1: Recognize need for programmable devices.

CO2 : Describe architecture of programmable devices..

CO3 : Explain programmable methodologies.

CO4 : Recall IC fabrication techniques vis-à-vis CMOS switch.

CO5: Relate design and implementation flow for PLDs.

CO6 : low power design techniques and methodologies.

Student Outcomes (SOs) from Criterion 3 covered by this Course

COs/SOs	a	b	c	d	e	f	g	h	i	j	k
CO1	H		M		M	M	M	H	M		L
CO2	M	L	H				H		L	H	
CO3	M	H	M				M	M	M		H
CO4	M	H	H		M				M		M
CO5		L			M	M	M		L		M
CO6				M	M	H	M				

List of Topics Covered

INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow – CMOS transistors- CMOS Design rules –Combinational logic Cell Sequential logic cell - Transistor as Resistors - Transistor parasitic capacitance – Logical effort - Library cell design – Library architecture.

PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Xilinx I/O blocks.

PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN 9

Entry: Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Low level design language - PLA tools EDIF- CFI design representation.

SILICON ON CHIP DESIGN 9

Voice over IP SOC - Intellectual Property – SOC Design challenges- Methodology and design-FPGA to ASIC conversion – Design for integration-SOC verification-Set top box SOC.

PHYSICAL AND LOW POWER DESIGN 9

Over view of physical design flow- tips and guideline for physical design- modern physical design techniques- power dissipation-low power design techniques and methodologies-low power design tools- tips and guideline for low power design.